Scrial No. 10/015,419 Response dated October 14, 2005 Reply to Office Action of August 24, 2005

Attorney Docket No. EN11348

## Amendments to the Claims:

- 1. (Currently Amended) An audio detection circuit comprising:
  - a. an audio signal;
- b. a circuit capable of converting the audio signal to a pulse train having a frequency proportional to that varies with a frequency of the audio signal; and
- c. an amplification circuit coupled to the circuit capable of converting the audio signal to a pulse train;

wherein the amplification circuit is actuated when the pulse train has a frequency above a predetermined threshold.

- 2. (Previously Presented) The circuit of claim 1, further comprising a logic array coupled between the circuit capable of converting the audio signal to a pulse train, the logic array having an enable control coupled to a clock signal having a predetermined frequency.
- 3. (Original) The circuit of claim 2, wherein the logic array comprises a ripple counter.

Serial No. 10/015,419
Response dated October 14, 2005
Reply to Office Action of August 24, 2005

Attorney Docket No. EN11348

- 4. (Currently Amended) An audio detection circuit comprising:
  - a. an audio signal;
- b. a means of comparing the audio signal to a threshold signal, wherein the means of comparing generates a pulse train having a frequency proportional to that varies with the audio signal;
- c. a logic array coupled to the means of comparing, the logic array having an enable control, wherein the logic array is responsive to the pulse train when the enable control is active;
- d. a clock signal having a predetermined frequency and duty cycle coupled to the cnable control of the logic array; and
- enable input, wherein the enable input is coupled to the logic array;

wherein the enable input of the amplifying means is actuated when the audio signal has a frequency component above a predetermined frequency threshold.

- 5. (Original) The circuit of claim 4, further comprising a delay circuit coupled to the enable input of the amplifying means.
- 6. (Original) The circuit of claim 5, wherein the logic array comprises a ripple counter.
- 7. (Original) The circuit of claim 6, wherein the ripple counter comprises at least two flip-flop circuits.
- 8. (Original) The circuit of claim 7, further comprising a loudspeaker coupled to the amplifying means.

Serial No. 10/015,419 Response dated October 14, 2005 Reply to Office Action of August 24, 2005 Attorney Docket No. EN11348

9. (Original) The circuit of claim 8, wherein the predetermined threshold is at least 217 Hz.

Attorney Docket No. EN11348

Serial No. 10/015,419 Response dated October 14, 2005 Reply to Office Action of August 24, 2005

- 10. (Original) An audio detection circuit comprising:
  - a. an audio signal;
  - b. a first amplifier coupled to the audio signal;
- c. a comparator having a reference voltage coupled to the first amplifier, wherein the comparator generates a pulse train proportional to the frequency of the audio signal;
- d. a ripple counter coupled to the comparator, the ripple counter having an enable control, wherein the ripple counter is responsive to the pulse train when the enable control is active;
- e. a clock having a predetermined frequency and duty cycle coupled to the enable control of the ripple counter; and
- f. a second amplifier having an enable input, the enable input being coupled to the ripple counter;

wherein the enable input of the second amplifier is actuated when the audio signal has a frequency component above a predetermined frequency threshold.